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(54) Parallel multi-phased amorphous silicon shift register for fast addressing of an amorphous silicon array

Amorphes Siliziumschiebmregister zur schnellen Addressierung eines amorphen Silizium Feldes

Registre à décalage en silicium amorphe, de type parallèle à multiphases pour l'adressage rapide d'un réseau en silicium amorphe

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Des ription

This inv ntion relates to a thin film transistor devic for driving a thin film transistor array. In particular, th driving device comprises a parallel multi-phased shift register and a multi-phased buffer combination for fast addressing select lines of a thin film transistor array, where the driving device is integrated with the array.

Amorphous silicon, (a-Si), thin film transistor technology has found numerous applications because of its low cost and processing compatibility with low temperature glass substrates which allows fabrication of large area systems. Circuits are regularly fabricated with linear dimensions in excess of 30cm. Thin film transistors, TFTs, are widely used as pixel addressing elements in large area active matrix liquid crystal displays, and in printing and scanning bars. Printing systems based upon lonography and Electrography have also been demonstrated with a-Si. An example of a typical electrographic writing head, manufacturable by thin film fabrication techniques, is fully disclosed in US-A-4 588 997. An example of a fabrication technique is also discussed in US-A-4 998 146.

EP-A-0 342 925 discloses an active matrix panel comprising a picture element matrix mounted on a transparent substrate. The panel includes a plurality of gate lines, a plurality of source lines, a plurality of picture elements, a gate line drive circuit and a source line drive circuit. Each of the picture elements includes a thin film transistor (TFT). Additionally, the gate line drive circuit and the source line drive circuit may also comprise a plurality of TFTs (see preamble of claim 1).

There are a variety of advantages to large area technology when it is applied to input or output devices. For many competing technologies some form of magnification is needed to scale up the system; for example laser printing or CCD scanning require optical magnification. Printing and scanning systems built in large area technology contain fewer mechanical and optical parts so the reliability can be higher. Moreover, with integrated electronic content on the input or output device, the number of interconnections may be reduced. Therefore, it would be advantageous to integrate more functionality onto a device whereby reducing the number of interconnects.

The technology for large area electronics is based in large part on an extension of crystal silicon integrated circuit technology; process modules of metal sputtering, photolithography, and chemical vapor deposition are still used. The substrate, however, can be a 32 cm x 34 cm rectangle of Corning 7059® glass as opposed to a 15 cm^2 slice from a crystalline silicon ingot. In the version of a-Si technology used for the devices in the print array there are three metal layers, a Chrome gate metal, a self aligned Chrome on N$^+$ source and drain, and an Aluminum interconnect. Th TFTs are in the inverted staggered structure and a passivation layer of silicon nitride is used over th TFT chann l. Polyimid is used for inter-metal isolation and for final passivation.

Th most striking feature of the drive characteristics of a-Si TFTs is the low output current. These transistors have both a low mobility and a large threshold voltage (1V to 2V). The mobility is nearly three orders of magnitude below crystal silicon. To partly compensate for the low drive current, higher operating voltages are used. The transistors can withstand V_{GS} (gate to source voltage) potentials up to 40 V without failure. However even with the higher drive voltage, the switching time is on the order of tens of microseconds.

The slow speed of a-Si TFTs can be offset by the fact that a-Si applications lend themselves to a high degree of parallelism. For instance in an electrographic writing head, each individual writing electrode has its own separate driving circuit and in theory all of the circuits can operate in parallel for the head to function. In reality however, the number of inputs needed to drive all the circuits in parallel makes this approach impossible. To reduce the inputs to a manageable number, a simple multiplexing scheme is used. In this scheme, the a-Si circuits are grouped into segments of driver circuits which share a common data bus for data input, and each circuit in a segment has a common select line. To load the entire device with data, each select line is enabled in turn loading the data present on the bus into the segment, one segment at a time.

Besides the speed, another complication is the threshold voltage shift. This is much faster in a-Si than in crystal silicon. Rises of up to 5V in an operational lifetime are seen and must be compensated for in the circuit design. Because of the higher threshold voltages and the slow speed of the TFTs, operating voltages are typically 15 V to 25 V. This complicates the input to large area circuits because level shifting buffers must be used. A large number of level shifters can add a significant cost to a system. It is therefore desirable to have as few inputs as possible thus reducing the number of level shifting buffers required. Such a reduction in input pads to an integrated circuit would decrease cost and typically increase reliability.

An illustrative device is a 11.84 inch, 400 driver per inch print array. The array has 32 parallel data drivers per segment, resulting in 148 segments; each being controlled by a single select line. Such a large number of inputs can drive up the cost of the array interface significantly, for reasons already discussed. There is opportunity to reduce the number of inputs even further by moving the select line drive circuitry directly into the a-Si array.

One method is to integrate into the array an a-Si serial-in/parallel-out shift register, whereby shifting a single active bit down the register enables each of the segments in turn. However, such an implementation may yield a device which is too slow for the needs of many arrays such as the electrographic writing head (e.g. 25kHz). What is needed is an a-Si shift r gister for driving a on dimensional print array integrated on the

same substrate as a-Si pixel drivers used for writing, which can operate at an increased sp ed. It would b advantageous to have a shift r gister design which could operate asily at an increased sp ed (e.g. 100kHz) and which reduces the number of select line inputs on a device (e.g. from 148 to 9), thereby representing a significant system cost reduction. US-A-4 466 020 shows the use of a shift register integrated on a combination read/write array. However, the shift register on that array is for loading image data, not for enabling segments of selected devices.

In accordance with the present invention, there is provided a shift register assembly comprising: an array of thin film transistor elements having a plurality of segments, each segment comprising N elements which are concurrently addressed by a common select line; a plurality of multi-phased dynamic shift register elements, each having an output signal for addressing a segment of N elements of the array; and a plurality of multi-phased buffers each having an input and an output, the input being connected to the output signal of a corresponding multi-phased dynamic shift register element, and the output providing drive capabilities for a corresponding common select line of the array, the select lines being sequentially activated during each phase of multi-phased operation.

In accordance with an embodiment of the present invention, the array is an electrographic writing head comprising a series of segments aligned in a linear array, each segment comprising a plurality of writing nibs and having a respective select line, the select lines being driven by a shift register assembly as described above.

By way of example only, an embodiment of the invention will be described with reference to the accompanying drawings.

In the drawings:

Figure 1 is a block diagram of a typical shift register/buffer configuration;

Figure 2 is a schematic of the dynamic shift register element and the buffer element used in Figure 1;

Figure 3 is a block diagram of a shift register/buffer configuration in accordance with the present invention utilizing the shift register element and buffer element of Figure 2;

Figure 4 is a timing diagram representing the clocks needed to drive the dynamic shift register/buffer configurations and the outputs of the buffer elements of Figures 1 and 2; and

Figure 5 is a schematic representation of an exemplary thirty-two bit segment of an integral thin film writing head utilizing the present invention.

As discussed above, integrating a shift register onto an a-Si array for th purpose of creating sequential select pulses can be advantageous. Referring to Figure 1, shown ar ight four-phased dynamic shift register el - ments 50, (SR_0-SR_7), connected in a traditional configuration, which can be used on an array to produce sequential select pulses. As seen in this traditional configuration, signal V_{IN} is shift d down the line of shift register elements such that the output f SR_0 feeds the input of SR_1, whose output feeds the input of SR_2, tc. In general, the output of one shift register element becomes the input of the next shift register element directly in line with it hence shifting the V_{IN} signal down the line. A four-phased shift register is depicted here having four clock inputs, C1, C2, C3, C4 needed for operation. The waveforms of these clock inputs can be seen in Figure 4. Note that clocks C1, C2, C3, and C4 are connected to the clock inputs C1, C2, C3, C4 of shift register 50 respectively. This clock connection is the same for each shift register element 50 shown in Figure 1.

As is known with four-phased dynamic shift registers, the output of shift register element 50 is valid only during two phases of the required four phases of the input clocks. When using the output of shift register element 50 as a select pulse, that output must be buffered to guarantee that the select signal V_{Gn} is always in a valid state and to provide enough driving current to drive several select lines. In this case, buffer element 60 is used to drive the resulting select signal. Detailed descriptions of four-phased dynamic shift register 50 and buffer 60 are described below.

Referring now to Figures 2 and 4, a typical four-phased ratioless shift register 50 design is shown which provides a large switching range and allows for fast operating speed since no pull-up devices are used. Four non-overlapping clock pulses, C_1, C_2, C_3, C_4 as seen in Figure 4, and represented during clock phases F_1 to F_4, are used to drive shift register element 50. As is known in the art, shift register element 50 works as follows: during clock phase F_1 the gate capacitance of TFT Q_H (between the gate of TFT Q_H and ground) is charged through TFT Q_1, this is the pre-charge phase; during clock phase F_2, TFT Q_2 is switched on, thus the gate capacitance of TFT Q_H will then be discharged or remain the same depending on the input to the gate of TFT Q_{IN}, this is the input sample phase; clock phases F_3 and F_4, are similar except that the output capacitance on the OUT line is pre-charged during F_3 and the state of TFT Q_H is sampled during F_4; and, after one cycle of the four-phased clocks, the input on the gate of TFT Q_{IN}, the IN signal, has been shifted to the output becoming the OUT signal. This OUT signal becomes the signal to be used as a sequential select line. It is important to note that the output bit state of the OUT signal is only valid during the F_1 and F_2 clock phases of the following cycle.

Buffer element 60 uses a two phase operation and is designed to sample the OUT signal of shift register element 50 only during a single phase. As discussed above, the OUT signal is valid only during two phases so buffer element 60 needs to sample this output signal only during the time the output of the shift register element is valid. When the output of the shift register ele-

m nt is not valid, th output of buffer element 60 must b valid but inactiv . Th select lin OUT or V_{Gn} is brought high by charging through TFT B_3 during phas F_2, and is held to ground by TFT B_4 during very phase except F_2, this is accomplished by connecting the gate of TFT B_4 to th complement of clock C2 (C2*). The reason for this grounding is to create a valid logic low output on the V_{Gn} line when the output of the shift register element is not valid.

During the F_1 phase, the output of shift register element 50 is sampled. If the valid output of shift register element 50 is low, the gate capacitance of B_3 is charged, causing the select line to be pulsed high during the F_2 phase. Buffer element 60 is an inverting buffer changing the input low to an output high. The charging through TFT B_3 is aided by the fact that when TFT B_3 is turned on, its gate is essentially floating (both TFT B_1 and TFT B_2 are off). Therefore the gate to drain capacitance of TFT B_3 causes the gate potential to bootstrap off of the rising F_2 pulse, maintaining a high gate to source potential during the charging. For the other case, where the valid output of shift register 50 is high, TFT B_3 is partially charged to the divided voltage between TFT B_1 and TFT B_2 during phase F_1. During the F_2 phase this node will continue discharging leaving TFT B_3 in a marginally on state, thus when clock C_2 goes high there will be some unwanted charging of the select line V_{Gn}. This problem can be overcome by making TFT B_4 sufficiently large so that when it switches off its gate to drain capacitance pulls the select line sufficiently negative to make this charging insignificant resulting in an output low signal.

If each shift register element and buffer element combination has a four-phased shift register element, then the output of buffer 60 becomes a pulse sequentially selecting the devices connected to the outputs of the shift register elements. As seen in Figure 4, this pulse or selection signal V_{Gn} occurs once per every four clock phases. Therefore, when using a four-phased shift register element in the traditional setup of Figure 1, the output of the shift register and buffer combination is valid only during one of the four phases. In other words, during three of the four phases there are no elements being selected.

Figure 3 shows eight four-phased dynamic shift register elements 50 (SR_0'-SR_7') with their respective buffer elements 60 (B_0'-B_7') having their inputs and outputs connected according to the present invention. As shown, the output of the first shift register element SR_0 provides the input to shift register element SR_4'. In the same manner, shift register element $SR_{1'}$ provides the input to shift register element SR_5', and so on. In this configuration, when using four-phased dynamic shift register elements, the output of one shift register element provides the input to the fourth shift register element down the line. Another notable difference between the configuration of Figure 3 from that of Figure 1 is in the way the clocks are connected to th clock inputs of shift register elements 50 and buffer elements 60. In the configuration of Figur 3, each shift r gister lement 50 is connected one quarter out of phase with the next consecutive or adjacent shift register element 50 in line.

F r example, the clock inputs C1, C2, C3, and C4 to shift register lement $SR_{0'}$ are connected to clocks C1, C2, C3, and C4 respectively. However, the clock inputs C1, C2, C3, and C4 to the next shift register element $SR_{1'}$ are connected to clocks C2, C3, C4, and Cl respectively and are one quarter out of phase with the clock inputs to SR_0'. Note also that the clock inputs to the buffer element associated with each shift register element are also one quarter out of phase with respect to the next buffer element in line. It is this "out of phase" clocking which provides for the increase in performance as will be discussed below.

The resulting outputs of the shift register system of Figure 3 are similar to that of the traditional long shift register of Figure 1, i.e. sequential select pulses. However, as will become apparent, using the multi-phased approach as described herein results in the ability to run a four-phased dynamic shift register system at four times the speed of the traditional setup. To the devices being selected, sequential select pulses are produced as with the traditional setup, but by running the shift register/buffer element combinations out of phase, the select pulses can be produced four times as fast because each of the four phases creates a select pulse which can be seen on Figure 4 with respect to signals V_{Gn}'.

For further illustration of this four-phased operation, refer to the description below and Figures 2, 3 and 4. In the timing diagram of Figure 4, when the input to the first four shift register elements, S_{R0}'-S_{R3}', (V_{IN}) goes low, each shift register element 50 will sample during different phases. It is the clock on input C2 which determines which phase the device will sample on. From the clock connections of Figure 3, it is shown that: SR_0' samples during F_2, SR_1' samples during F_3, SR_2' samples during F_4, and SR_3' samples during F_1 of the next group of phases. During the next four phases of the clocks this input data will be shifted to the output of each shift register element 50. The output of each shift register element will be valid during only two phases. For SR_0' the output will be valid during phases F_1 and F_2 in cycle B, for SR_1' the output will be valid during phases F_2 and F_3 in cycle B, for SR_2' the output will be valid during phases F_3 and F_4 in cycle B, and for SR_3' the output will be valid during phases F_4 and F_1 in cycles B and C respectively. As already described, buffer element 60 will sample during the phases when the shift register element output is valid, delivering its boosted signal during the second of the two. Therefore select line V_{G0}' is enabled during F_2 of cycle B, since buffer element B_0' is sampling a valid output during F_1. V_{G1}' is enabled during F_3 of cycle B, V_{G2}' is enabled during F_4 of cycle B, and $V_{G3'}$ is enabled during F_1 of cycle C. This cycle will repeat with the next four select lines nabl d from F_2 of cycle C to F_1 of cycle D and so forth, until all of the r quired select lines on a device are enabled. It is the clock which is connected to

th C2 inputs of the buffer elements which determines which phase the select lines will be enabled n.

As already stated, charging and discharging through a-Si TFTs typically takes about 10 microseconds, th refore since each phase in th shift register operation involves charging through a TFT, a combination four-phased shift register 50 with a buffer 60 as seen in Figure 1 has an operating frequency of 25kHz. However, since the output of the buffer 60, V_{Gn}, only occurs during one of the four phases (F_2), and since the sole purpose of shift register 50 is to shift a single active bit down the line of shift register elements creating sequential select pulses, the speed at which these select pulses are produced can be improved by a factor of four. As can be seen from the timing diagram of Figure 4, there is a select pulse V_{Gn}' from the shift register and buffer configuration of Figure 3 during each clock phase so that, the select lines are active during each phase of the multiphased clock giving an effective shift register speed of 100kHz. In other words, V_{Gn} is active during F_2 of B, F_2 of C, F_2 of D and F_2 of E whereas V_{Gn}' is active during F_2 of B, F_3 of B, F_4 of B F_1 of C and F_2 of C.

The combination parallel shift register and buffer operation needs a complement of each of the four clock inputs, C1*, C2*, C3*, C4*, bringing the number of clock inputs to eight. However, only one shift register input V_{IN} is needed since a single line can be used to start the first four parallel shift register elements at the beginning of the line of shift register elements. Since each of the parallel shift register elements only sample their input during their respective sample phases, to start a line the shift register input V_{IN} just needs to be pulsed low during the first occurrences of phases F_2,F_3,F_4, and F_1 as shown in Figure 4.

Referring now to Figure 5, shown is a thirty-two bit segment of a electrographic writing head utilizing the present invention. Several of these thirty-two bit segments can be aligned in a linear array making a full width writing head. Each of the thirty-two bit segments is sequentially selected by a single V_{Gn} pulse created by the shift register/buffer configuration shown in Figure 3. Although an electrographic writing head is used as an example of where the shift register/buffer configuration can be utilized, it can be appreciated that the configuration could be used to drive many types of TFT arrays as discussed above.

In general, the output of buffer 60, selection signal V_G, drives a group of thirty-two Random Access Memory (RAM) cells 70 concurrently. In order to provide adequate current drive for charging the gate capacitance of the group of static ram cells 70 (typically about 10pF) and to provide all known states for select line V_G, buffer 60 is utilized between the output bit of shift register element 50 and the gate select line, V_G of RAM cell 70. The pulse delivered by the buffer 60 is inverted from the output of shift register 50, therefor a line time is accomplished by shifting a single active bit 0 (low) down shift register 50 rather than shifting a bit 1 (high). Once all RAM c lls 70 in each thirty-two bit segment of array 10 ar loaded, a writ pulse, V_W is given to all latch cells 80 latching the data from RAM cells 70 onto latch c lls 80. With the latching of th data, th data on latch c lls 80 is then simultaneously transferred t nibs 12 through cascod circuit 90 for writing onto a medium. As stated, an electrographic writing head is only one example of where the present invention can be utilized.

A four-phased multi-phased shift register configuration has been described above. However, one can envision a multi-phased shift register configuration having M phases. A plurality of multi-phased dynamic shift registers arranged in a linear array can be divided into blocks of M shift register elements. The output signal from each of the plurality of multi-phased dynamic shift register elements in a block of M is connected to an input of a corresponding multi-phased dynamic shift register element in a next consecutive block of M shift register elements. This configuration implies that the shift register elements within a block of M would be operated 1/M out of phase with each other.

In other words, in the particular case where M is equal to four (as illustrated in Fig. 3), each shift register element is a four-phased shift register element. A linear array of four-phased shift register elements is divided up into blocks of four four-phased shift register elements. The output of the first shift register element in a first block of four shift register elements drives the input to the first, or corresponding, shift register element in a next block of four shift register elements. In a similar manner, the output of the second shift register element in the first block of four shift register elements drives the input to the corresponding second shift register element in the next block of four shift register elements.

Another example of a device which can utilize the approach described above is an amorphous Silicon active matrix display. For instance, for a display with 1024 columns by 1024 rows, a multi-phased shift register device in accordance with the invention can be used for the row selection. If this display is to have a frame rate of 60Hz, this would require a line time of 16 microseconds, well within the speed of the shift register's operation, and the number of inputs for the row drivers would be reduced from 1024 to 9.

As can be appreciated, a shift register assembly in accordance with the present invention could be utilized by many types of TFT arrays. Although an a-Si device is described above, it can be appreciated that the device could be made from non-crystalline silicon (e.g. polycrystalline, micro-crystalline).

Claims

1. A shift register assembly comprising:

an array of thin film transistor elements having a plurality of segments, each segment compris-

ing N el m nts (70) which are concurrently addressed by a common select line;

a plurality of multi-phased dynamic shift regist r elem nts (50; SR_0', SR_1', SR_2', SR_3', SR_4', SR_5', SR_6', SR_7'), each having an output signal for addressing a segment of N elements of the array; and

a plurality of buffers (60; B_0', B_1', B_2', B_3', B_4', B_5', B_6', B_7') each having an input and an output, the input being connected to the output signal of a corresponding multi-phased dynamic shift register element (50; SR_0', SR_1', SR_2', SR_3', SR_4', SR_5', SR_6', SR_7'), and the output providing drive capabilities for a corresponding common select line of the array, the select lines being sequentially activated during each phase of multi-phased operation,

characterized in that the buffer are multi-phased buffers.

2. An assembly according to claim 1, wherein the plurality of multi-phased dynamic shift register elements are divided into blocks (SR_0', SR_1', SR_2', SR_3'; SR_4', SR_5', SR_6', SR_7') aligned consecutively in a linear array, each block having M shift register elements, where M equals the number of phases.

3. An assembly according to claim 2, wherein each multi-phased dynamic shift register element (50; SR_0', SR_1', SR_2', SR_3', SR_4', SR_5', SR_6', SR_7') is operated 1/M out of phase with a next multi-phased dynamic shift register element.

4. An assembly according to claim 3, wherein the output signal from each multi-phased dynamic shift register element (50; SR_0', SR_1', SR_2', SR_3') in each block is connected to an input of a corresponding multi-phased dynamic shift register in a next consecutive block of shift register elements (50; SR_4', SR_5', SR_6', SR_7').

5. An assembly according to any one of claims 2 to 4, wherein the output of the multi-phased buffer is active only during one phase of multi-phased operation.

6. An assembly according to any one of claims 2 to 5, wherein clock inputs (C1, C2, C3, C4) to each of the shift register elements (SR_0', SR_1', SR_2', SR_3'; SR_4', SR_5', SR_6', SR_7') in a block are 1/M out of phase with one another.

7. An assembly according to any one of claims 2 to 6, wherein M is equal to four.

8. A shift r gist r assembly according to any one of the preceding claims, wherein th elem nts are writing nibs (12) of an lectrographic writing head.

Patentansprüch

1. Schieb registerv rrichtung mit:

einem Feld aus Dünnfilmtransistorelementen mit einer Vielzahl von Segmenten, wobei jedes Segment N Elemente (70) umfaßt, die gleichzeitig von einer gemeinsamen Anwählleitung adressiert werden;

einer Vielzahl von dynamischen Mehrphasen-Schieberegisterelementen (50, SR_0', SR_1, SR_2', SR_3', SR_4', SR_5', SR_6', SR_7'), von denen jedes ein Ausgangssignal zum Adressieren eines Segmentes von N Elementen des Feldes hat; und

einer Vielzahl von Puffern (60, B_0', B_1', B_2', B_3', B_4', B_5', B_6', B_7'), von denen jeder eine Eingangsgröße und eine Ausgangsgröße hat, wobei die Eingangsgröße an das Ausgangssignal eines entsprechenden dynamischen Mehrphasen-Schieberegisterelements (50, SR_0', SR_1, SR_2', SR_3', SR_4', SR_5', SR_6', SR_7') angeschlossen ist und die Ausgangsgröße die Ansteuerung einer entsprechenden gemeinsamen Anwählzeile des Feldes ermöglicht, wobei die Anwählzeilen nacheinander während jeder Phase des Mehrphasenvorgangs aktiviert werden,

gekennzeichnet dadurch, daß es sich bei den Puffern um Mehrphasenpuffer handelt.

2. Vorrichtung gemäß Anspruch 1, wobei die Vielzahl der dynamischen Mehrphasen-Schieberegisterelemente in Blöcke (SR_0', SR_1, SR_2', SR_3', SR_4', SR_5', SR_6', SR_7) untergliedert sind, die nacheinander in einer linearen Anordnung ausgerichtet sind, und wobei jeder Block M Schieberegisterelemente aufweist und M mit der Anzahl der Phasen identisch ist.

3. Vorrichtung gemäß Anspruch 2, wobei jedes dynamische Mehrphasen-Schieberegisterelement (50, SR_0', SR_1, SR_2', SR_3', SR_4', SR_5', SR_6', SR_7') um 1/M phasenverschoben zu einem nächsten dynamischen Mehrphasen-Schieberegisterelement betrieben wird.

4. Vorrichtung gemäß Anspruch 3, wobei das Ausgangssignal aus jedem dynamischen Mehrphasen-Schieberegisterelement (50, SR_0', SR_1, SR_2', SR_3') in jedem Block an den Eingang eines entsprechenden dynamischen Mehrphasen-Schieberegisterelements in einem nächsten, anschließenden Block von Schieber gisterelementen (50, SR_4', SR_5', SR_6', SR_7') angeschlossen ist.

5. Vorrichtung gemäß inem der Ansprüch 2 bis 4, wobei di Ausgabe des Mehrphasenpuffers nur während einer Phas d s Mehrphasenv rgangs aktiv ist.

6. Vorrichtung gemäß einem der Ansprüche 2 bis 5, wobei die Takteingaben (C1, C2, C3, C4) in jedes der Schieberegisterelemente (SR_0', SR_1, SR_2', SR_3', SR_4', SR_5', SR_6', SR_7') in einem Block zueinander um 1/M phasenverschoben sind.

7. Vorrichtung gemäß einem der Ansprüche 2 bis 6, wobei M gleich vier ist.

8. Schieberegistervorrichtung gemäß einem der vorangehenden Ansprüche, wobei die Elemente Schreibspitzen (12) eines elektrografischen Schreibkopfes sind.

Revendications

1. Ensemble de registres à décalage comprenant :

   une matrice d'éléments de transistor à couche mince comportant une pluralité de segments, chaque segment comprenant N éléments (70) qui sont simultanément adressés par une ligne de sélection commune ;
   une pluralité d'éléments de registre à décalage dynamique à phases multiples (50 ; SR_0', SR_1', SR_2', SR_3', SR_4', SR_5', SR_6', SR_7'), ayant chacun un signal de sortie pour adresser un segment parmi les N éléments de la matrice ; et
   une pluralité de tampons (60 ; B_0', B_1', B_2', B_3', B_4', B_5', B_6', B_7') ayant chacun une entrée et une sortie, l'entrée étant connectée au signal de sortie de chaque elément de registre à décalage dynamique à phases multiples correspondant (50 ; SR_0', SR_1', SR_2', SR_3', SR_4', SR_5', SR_6', SR_7') et la sortie procurant des capacités d'attaque pour une ligne de sélection commune correspondante de la matrice, les lignes de sélection étant séquentiellement activées pendant chaque phase de l'opération à phases multiples,

   caractérisé en ce que les tampons sont des tampons multiphases.

2. Ensemble selon la revendication 1, dans lequel le pluralité des éléments de registre à décalage dynamique à phases multiples sont divisés en blocs (SR_0', SR_1', SR_2', SR_3', SR_4', SR_5', SR_6', SR_7') alignés consécutivement en une rangée, chaque bloc ayant M éléments de registre à décalage, où M est égal au nombre de phases.

3. Ens mble selon la rev ndication 2, dans lequ l chaque élément de registre à décalage dynamique à phases multiples (50 ; SR_0', SR_1', SR_2', SR_3', SR_4', SR_5', SR_6', SR_7') est mis en oeuvre déphasé d 1/M par rapport à un élément de registre à décalage dynamique à phases multiples suivant.

4. Ensemble selon la revendication 3, dans lequel le signal de sortie de chaque élément de registre à décalage dynamique à phases multiples (50 ; SR_0', SR_1', SR_2', SR_3') dans chaque bloc est connecté à une entrée d'un registre à décalage dynamique à phases multiples correspondant dans un bloc consécutif suivant des éléments de registre à décalage (50 ; SR_0', SR_4', SR_5', SR_6', SR_7').

5. Ensemble selon l'une quelconque des revendications 1 à 4, dans lequel la sortie du tampon à phases multiples est active seulement pendant une phase de l'opération multiphases.

6. Ensemble selon l'une quelconque des revendications 2 à 5, dans lequel les entrées d'horloge (C1, C2, C3, C4) dans chacun des éléments de registre à décalage (SR_0', SR_1', SR_2', SR_3', SR_4', SR_5', SR_6', SR_7') dans un bloc sont déphasés de 1/M entre-elles.

7. Ensemble selon l'une quelconque des revendications 2 à 6, dans lequel M est égal à quatre.

8. Ensemble de registres à décalage selon l'une quelconque des revendications précédentes, dans lequel les éléments sont des plumes d'écriture (12) d'une tête d'écriture électrographique.

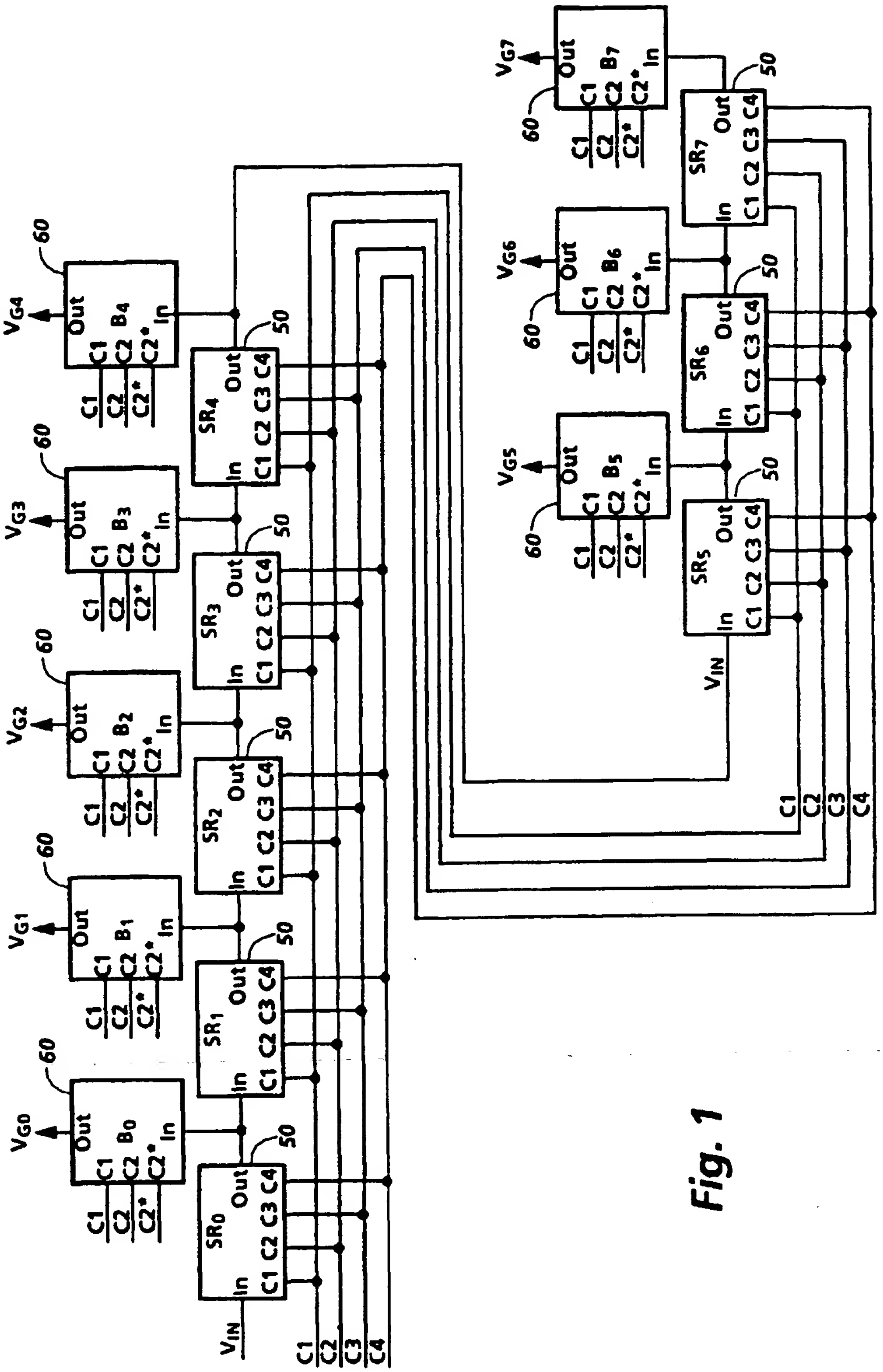

SR0
SR1
SR2
SR3
SR4
SR5
SR6
SR7
B0
B1
B2
B3
B4
B5
B6
B7
VG0
VG1
VG2
VG3
VG4
VG5
VG6
VG7
VIN
In
Out
C1 C2 C3 C4
C1
C2
C2*
50
60

Fig. 1

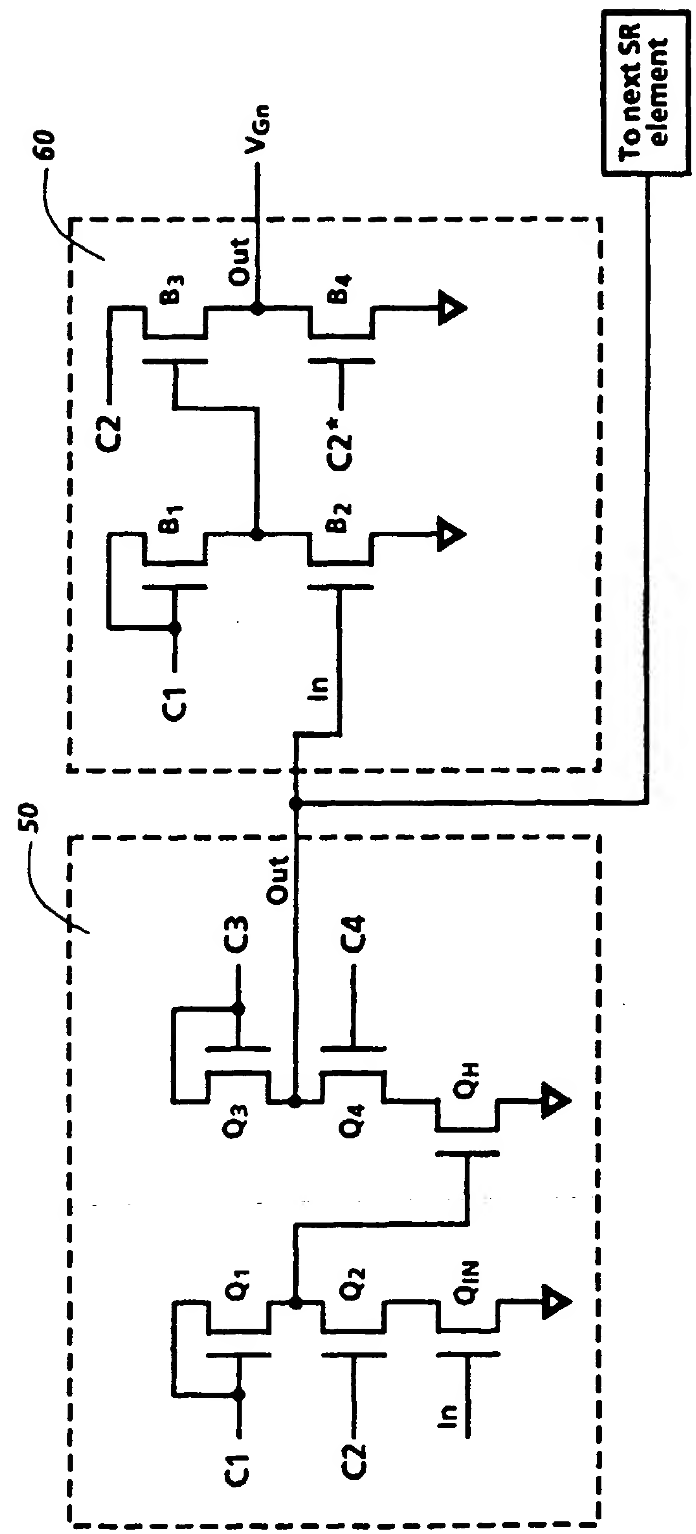
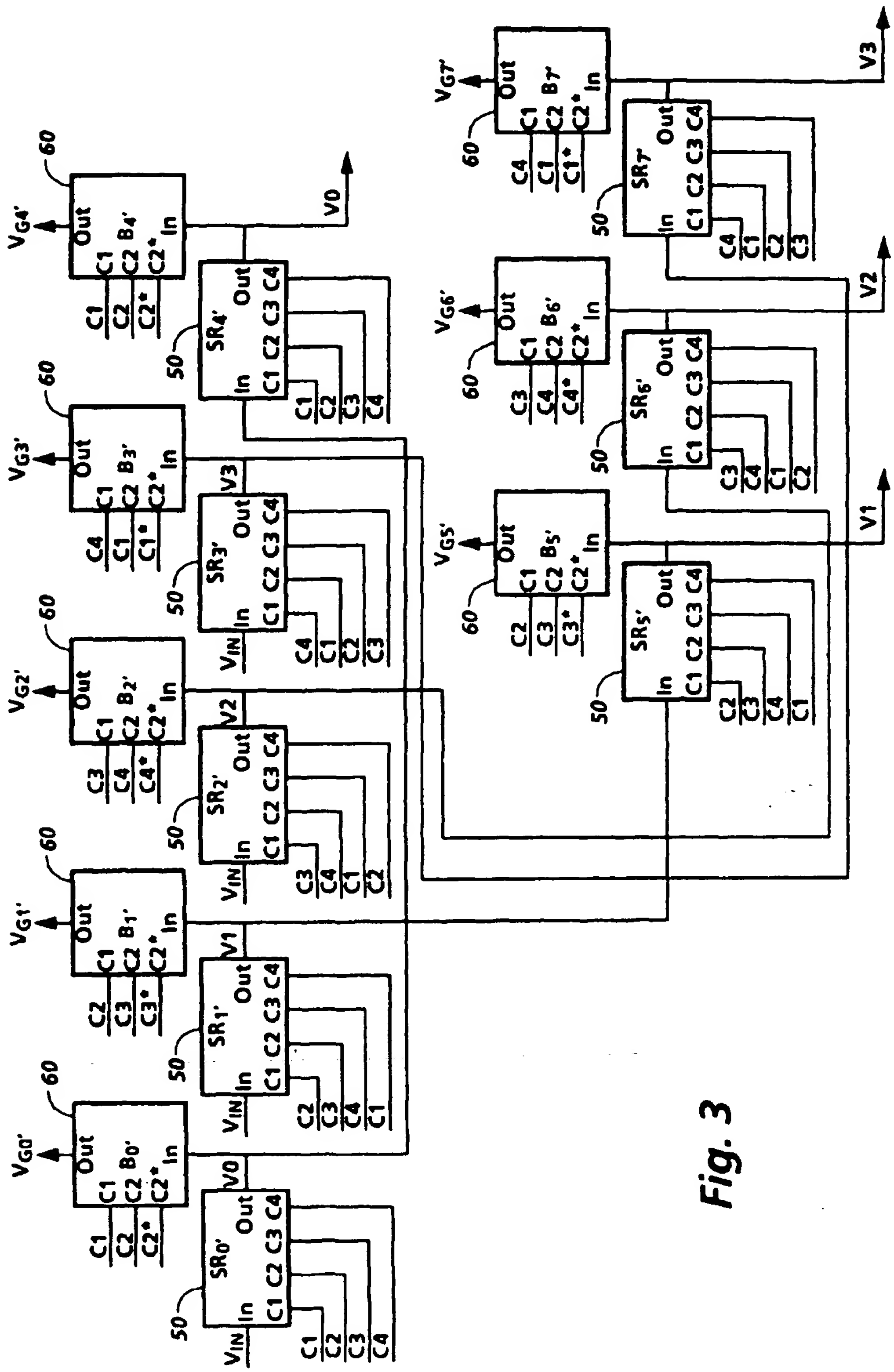

60
V_{Gn}
To next SR element
Out
B_3
B_4
C2
C2*
B_1
B_2
C1
In
50
Out
C3
C4
Q_3
Q_4
Q_H
Q_1
Q_2
Q_{IN}
C1
C2
In

Fig. 2



SR0'
SR1'
SR2'
SR3'
SR4'
SR5'
SR6'
SR7'
B0'
B1'
B2'
B3'
B4'
B5'
B6'
B7'
VG0'
VG1'
VG2'
VG3'
VG4'
VG5'
VG6'
VG7'
VIN
V0
V1
V2
V3
50
60

Fig. 3

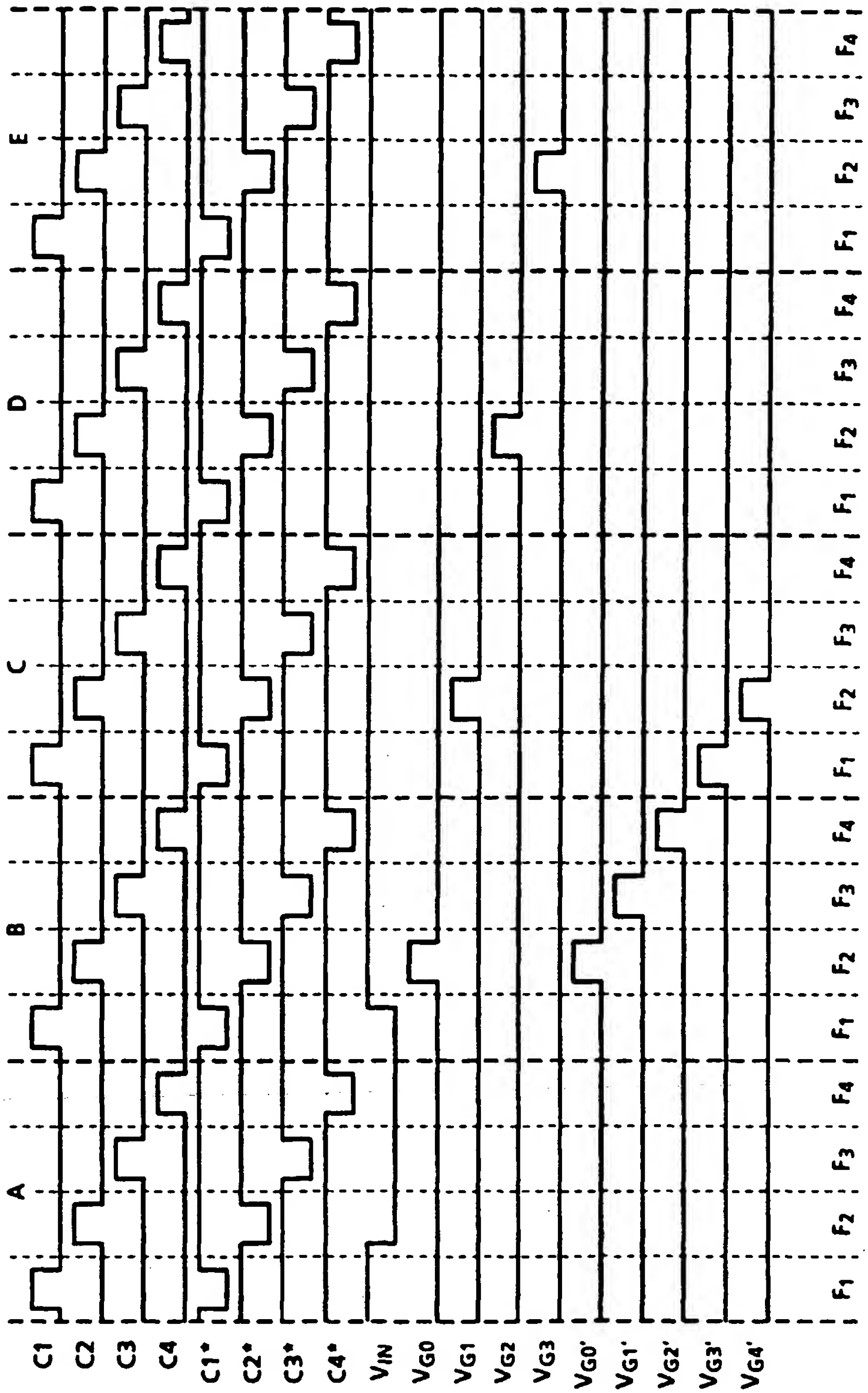

A
B
C
D
E
F1 F2 F3 F4
C1
C2
C3
C4
C1*
C2*
C3*
C4*
V_IN
V_G0
V_G1
V_G2
V_G3
V_G0'
V_G1'
V_G2'
V_G3'
V_G4'

Fig. 4

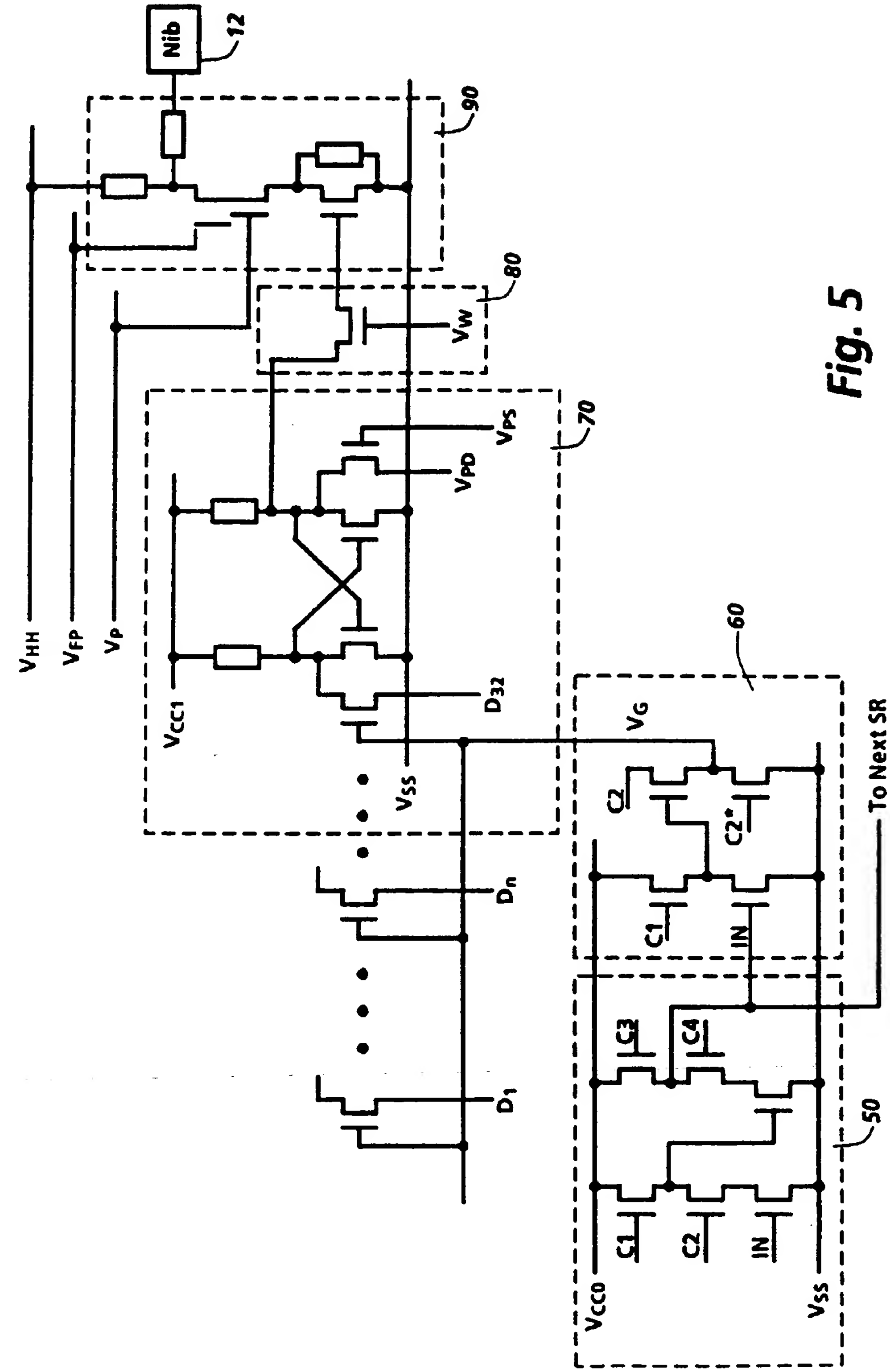

Nib
12
90
80
V_W
70
V_{PS}
V_{PD}
V_{HH}
V_{FP}
V_P
V_{CC1}
D_{32}
V_{SS}
D_n
D_1
60
V_G
C2
C2*
C1
IN
C3
C4
To Next SR
50
C1
C2
IN
V_{CC0}
V_{SS}

Fig. 5